CLAIMS

What is claimed is:

1. A method of protecting a transistor gate structure during a selective epitaxial deposition process, the method comprising:

forming silicon germanium oxide above a gate structure;

performing a selective epitaxial deposition process while the silicon germanium oxide is above the gate structure; and

removing the silicon germanium oxide after the selective epitaxial deposition process.

2. The method of claim 1, wherein forming silicon germanium oxide above a gate structure comprises:

forming silicon germanium over a gate material layer; and

oxidizing the silicon germanium to form silicon germanium oxide over the gate material layer.

3. The method of claim 2, further comprising patterning the silicon germanium and the gate material layer before oxidizing the silicon germanium.

4. The method of claim 3, further comprising forming a sidewall spacer along a lateral side of the patterned gate material layer after patterning the silicon germanium and the gate material layer and before oxidizing the silicon germanium.

5. The method of claim 4, wherein patterning the silicon germanium and the gate material layer exposes a portion of a semiconductor body onto which epitaxial material is to be deposited, wherein oxidizing the silicon germanium forms silicon germanium oxide over the gate material layer and forms an oxide material over the exposed portion of the semiconductor body, further comprising performing a clean operation prior to performing the selective epitaxial deposition process, the clean operation removing the oxide material

from the semiconductor body and leaving silicon germanium oxide over the gate material layer.

6. The method of claim 5, further comprising removing a portion of the exposed semiconductor body to form a recess after performing the clean operation and prior to performing the selective epitaxial deposition process.

7. The method of claim 6, wherein the semiconductor body comprises silicon, wherein the gate material layer comprises polysilicon, and wherein performing the selective epitaxial deposition process comprises forming epitaxial silicon in the recess of the semiconductor body while the silicon germanium oxide is above the gate structure.

8. The method of claim 5, wherein the semiconductor body comprises silicon, wherein the gate material layer comprises polysilicon, and wherein performing the selective epitaxial deposition process comprises forming epitaxial silicon over the semiconductor body while the silicon germanium oxide is above the gate structure.

9. The method of claim 3, wherein patterning the silicon germanium and the gate material layer exposes a portion of a semiconductor body onto which epitaxial material is to be deposited, wherein oxidizing the silicon germanium forms silicon germanium oxide over the gate material layer and forms an oxide material over the exposed portion of the semiconductor body, further comprising performing a clean operation prior to performing the selective epitaxial deposition process, the clean operation removing the oxide material from the semiconductor body and leaving silicon germanium oxide over the gate material layer.

10. The method of claim 9, further comprising removing a portion of the exposed semiconductor body to form a recess after performing the clean operation and prior to performing the selective epitaxial deposition process.

11. The method of claim 9, wherein the semiconductor body comprises silicon, wherein the gate material layer comprises polysilicon, and wherein performing the selective epitaxial deposition process comprises forming epitaxial silicon over the semiconductor body while the silicon germanium oxide is above the gate structure.

12. The method of claim 2, wherein the gate material layer comprises polysilicon, and wherein performing the selective epitaxial deposition process comprises forming epitaxial silicon over a semiconductor body while the silicon germanium oxide is above the gate structure.

13. The method of claim 1, wherein the gate structure comprises polysilicon, and wherein performing the selective epitaxial deposition process comprises forming epitaxial silicon over a semiconductor body while the silicon germanium oxide is above the gate structure.

14. A method of forming a protection structure over a transistor gate structure, the method comprising:

forming silicon germanium above a gate material layer;

selectively etching the silicon germanium and the gate material layer to form a patterned gate structure;

oxidizing the silicon germanium and an exposed portion of a semiconductor body to form silicon germanium oxide over the gate structure and an oxide over the exposed portion of the semiconductor body;

removing the oxide material from the semiconductor body without removing all of the silicon germanium oxide;

performing a selective epitaxial deposition process while the silicon germanium oxide is above the gate structure; and

removing the silicon germanium oxide after the selective epitaxial deposition process.

15. The method of claim 14, further comprising recessing an exposed portion of the semiconductor body after removing the oxide material from the semiconductor body and prior to performing the selective epitaxial deposition process.

16. A method of fabricating a transistor, the method comprising:

forming a gate dielectric layer above a semiconductor body;

forming a gate electrode layer above the gate dielectric layer;

forming a protection layer above the gate electrode layer;

selectively etching the protection layer and the gate electrode layer to form a patterned gate structure and to expose a portion of the semiconductor body;

oxidizing the protection layer and an exposed portion of the semiconductor body to form a first oxide material on the patterned gate structure and a second oxide material on the exposed portion of the semiconductor body;

performing a first clean operation to remove the second oxide material from the semiconductor body, the first clean operation leaving at least a portion of the first oxide material on the patterned gate structure;

performing a selective semiconductor material deposition process with the first oxide material on the patterned gate structure, the deposition process forming a semiconductor material on the exposed portion of the semiconductor body and substantially no semiconductor material on the first oxide material on the patterned gate structure; and

performing a second clean operation to remove the first oxide material after the deposition process.

17. The method of claim 16, wherein forming the gate electrode layer comprises depositing polysilicon above the gate dielectric layer.

18. The method of claim 16, wherein forming a protection layer comprises forming silicon germanium above the gate dielectric layer.

19. The method of claim 18, wherein oxidizing the protection layer comprises forming silicon germanium oxide on the patterned gate structure.

20. The method of claim 16, further comprising recessing an exposed portion of the semiconductor body after performing the first clean operation and prior to the selective semiconductor material deposition process.